REMARKS

The following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 102(e) Rejections

Examiner rejected claims 1, 2, 4-20, 22-35, and 37-67 as being anticipated by U.S. Patent No. 6,088,370 (hereinafter referred to as Bell).

> "To anticipate a claims, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Independent claims 1, 16, 29, 30, 47, and 50 of the present application includes limitations not disclosed or taught by the Bell. As a result, the independent claims 1, 16, 29, 30, 47, and 50 are not anticipated by the Bell.

In particular, the independent claims include the limitation of an interface "between a memory control hub (MCH) and a input/output control hub (ICH)".

Bell, however, does not disclose an interface between a memory control hub (MCH) and a input/output control hub (ICH). Rather, Bell only discloses a bus system that provides "connections between a controller 115, which functions as a bridge between a microprocessor bus 110, to which one or more microprocess devices are connected . . . and bus expander bridges 117, 120, and 125." (Bell Col. 2, lns. 21-27).

More specifically, according to the examiner, the controller 115 as shown in Bell discloses applicant's claimed MCH. The examiner further states that one of the bus expander bridges 117, 120, and 125 as shown in Bell disclose applicant's claimed input/output control hub (ICH). Applicant respectfully disagrees.

The bus expander bridges 117, 120, and 125 shown and described in Bell, do not disclose applicant's claimed input/output control hub (ICH). As defined in applicant's detailed description, the ICH is a hub that is capable of providing an interconnection between various peripheral components and external buses, with a separate bus interface.

The expander bridges as shown in Bell are different than the input/output control hub as claimed by applicant in that the expander bridges have more limited capability. The expander bridges are unable to accept/interconnect multiple peripherals and external buses with another interface or bus. As a result, multiple expander bridges need to be used to provide the function or service of the claimed input/output control hub.

Specifically, see Figure 1 and accompanying description of Bell. As shown and described in Bell, multiple expander bridges 117, 120, and 125 are shown to interface the controller 115, compared to applicants claimed input/output control hub interfacing with the claimed MCH. The disadvantages of using the expander bridges rather than the claimed input/output control hub, include the resulting increase in signal and data paths that results from having multiple expander bridges interconnected with the controller 115, compared to the input/output control hub interface with the MCH.

For example, as shown and described in Figure 1 of Bell, there are at least 4 separate interconnections between bridges and the controller 115, resulting in at least four different 16 bit busses/interfaces to the controller 115. To the contrary, applicant's claimed input/output control hub results in significantly more simple interconnection than the use of the multiple bridges as shown in Bell. By way of exemplary embodiment only, as shown in applicant Figure 8 of applicant's detailed description, the interface of the input/output control hub to the MCH, includes the simple interface of only a 25 bit signal path (the actual size of an interface between an ICH and MCH may vary within the scope of the invention).

Therefore, considering the multiple expander bridges disclosed in Bell are clearly distinct and separate from the claimed input/output control hub as claimed by applicant, Bell clearly does not anticipate applicants' independent claims.

In addition, applicants' remaining claims depend from at least one of the independent claims mentioned above. As a result of depending from one of the independent claim, the remaining claims include the distinguishing limitations discussed above, and are therefore also not anticipated by Bell.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 09/20/2002

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ATTACHMENT A

A marked-up version of Page 2, line 7 of the Specification is as follows:

The present invention relates to the field of computer systems, and, in particular, the field of providing an improved interface between computer components. This continuing prosecution application is a continuation under 37 C.F.R. 1.53(d) of prior application no. 09/428,134 filed on 10/26/1999, entitled METHOD AND APPARATUS FOR AN IMPROVED INTERFACE BETWEEN COMPUTER COMPONENTS, which is a continuation in part of application no. 09/186,219 filed 11/03/1998.